FIG. 26 shows a lateral conductivity modulation type MOSFET formed on a substrate obtained by forming the N^- type epitaxial layer 202 having a low impurity density on a P substrate. In this embodiment, the N type diffusion layer 230 is formed to partially overlap the P base layer 204. With such an arrangement, a lateral resistance of the N^- type epitaxial layer 202 formed immediately under the P base layer 204 can be kept small. In addition, by additionally forming the N type diffusion layer 230, an impurity density of a wafer surface portion is decreased. Therefore, the channel region CH of the P base layer 204 can be decreased, as shown in FIG. 26. As a result, a lateral resistive component of the P base layer 204 can be further decreased, and a channel resistance can also be reduced. This contributes to a phenomenon of the turn-on voltage of the element. When an impurity dose in a depth direction per unit wafer area (i.e., an integral value of the impurity density in a wafer depth direction) of a part of the epitaxial layer 202 having a low impurity density located between the P base layer 204 and the N type drain isolating layer 208 is set to be 2×10^{12} ions/cm^2 or less, and that of the N type diffusion layer 230 is set to be substantially equal to the above value, the withstand voltage of the element can be maximized.

What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate;

a conductivity-modulation field effect transistor formed on said substrate, said transistor having a base region of a first conductivity type, a source region of a second conductivity type formed in one portion of said base region, a source electrode for electrically connecting said base region and said source region with each other, a drain region of the first conductivity type formed in another portion of said base region, a drain electrode formed on said drain region, and a gate electrode insulatively provided above said substrate on a channel region formed between source and drain regions; and

means for, when said transistor is turned off, facilitating carriers in said device to flow into said drain electrode, thereby accelerating dispersion of the carriers in said transistor, said means comprising a first heavily-doped semiconductive layer of the second conductivity type which is formed in said drain region to have a conductivity type opposite to that of said drain region, said semiconductive layer being in contact with said drain electrode.

2. The device according to claim 1, wherein said substrate has a surface in which said base region an said drain region are formed.

3. The device according to claim 2, further comprising:

a second heavily-doped semiconductive layer which is formed in said drain region to overlap the first heavily-doped semiconductive layer, said second semiconductive layer having a conductivity type opposite to that of said first semiconductive layer.

4. The device according to claim 2, further comprising:

a second heavily-doped semiconductive layer which is formed in said drain region to be contact with said drain electrode, said second semiconductive layer having a conductivity type opposite to that of said first semiconductive layer.

5. The device according to claim 4, further comprising:

a third heavily-doped semiconductive layer having the conductivity type opposite to that of said source region and which is formed in said substrate so as to overlap said base region and said source region and to be in contact with said source electrode.

6. A single-gate type conductivity-modulation field effect transistor comprising:

a first base layer having a surface;

a second base layer of a first conductivity type provided in the surface of said first base layer;

a source layer provided in said second base layer;

a source electrode provided on the layer surface, for electrically shorting said second base layer with said source layer;

a drain layer having said first conductivity type provided in said layer surface;

a drain electrode formed on said layer surface to be in contact with said drain layer;

a gate electrode insulatively provided above said layer surface, for covering a certain surface portion of said second base layer which is positioned between said first base layer and said source layer to define a channel region below said gate electrode; and

a heavily-doped semiconductor layer of a second conductivity type which is provided in a selected surface portion of said drain layer and which is included in said drain layer to be in contact with said drain electrode, said heavily-doped semiconductor layer facilitating, when said transistor is turned off, carriers accumulated in said first base layer to flow into said drain electrode through said drain layer, thereby accelerating dispersion of the carriers in said transistor; and

wherein said first base layer and said source layer have said second conductivity type.

7. The transistor according to claim 6, wherein said drain layer comprises heavily-doped drain layer portions each pair of two adjacent layer portions of which are separated from each other.

8. The transistor according to claim 7, wherein said source layer has one side portion along which a plurality of projected layer portions are aligned to define a comb-shaped planar pattern.

9. The transistor according to claim 6, further comprising:

a high-resistive layer insulating provided above said layer surface and connected with said source electrode and said drain electrode.

10. The transistor according to claim 6, wherein said drain layer comprises:

a first diffusion layer; and

a second diffusion layer which at least partially surrounds said heavily doped semiconductor layer and which has its depth smaller than that of said first diffusion layer, said second diffusion layer formed adjacent said first diffusion layer.

11. The transistor according to claim 10, further comprising:

a second heavily doped semiconductor layer of a conductivity type which is the same of that of said drain layer and which is formed in said first diffusion layer.

12. The transistor according to claim 11, wherein said second heavily doped semiconductor layer is in contact with said drain electrode.

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